IN THE CLAIMS

Please cancel claims 9, 17 and 20-26 without prejudice. Please amend the remaining claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) An integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the processor; and

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps,

wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface, and

wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins, and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

2. (Previously Presented) An integrated circuit according to claim 1, which comprises a mode setting pin for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

3. (Previously Presented) An integrated circuit according to claim 1, wherein said request directing unit comprises switching means responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

4. (Previously Presented) An integrated circuit according to claim 3, wherein said switching means comprises a multiplexer.

5. (Previously Presented) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory mapped peripheral.

6. (Previously Presented) An integrated circuit according to claim 1, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

7. (Currently Amended) An integrated circuit ~~according to claim 1,~~ comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the processor; and

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps,

wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in said second memory address map said first range of addresses are also allocated to the interface, which comprises control registers addressable in said memory space, wherein in said first memory address map said first range of addresses include addresses of control registers associated with said at least one resource and in said second address map said addresses are reallocated to control registers associated with the interface.

8. (Previously Presented) An integrated circuit according to claim 2, wherein said mode is set by application of a logic value selected from one and zero on the mode setting pin.

Claim 9 (Canceled).

10. (Currently Amended) An integrated circuit according to claim ~~9~~ 1, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

11. (Previously Presented) An integrated circuit according to claim 10, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

12. (Currently Amended) A prototype system comprising an integrated circuit comprising:

a processor operable to issue memory access requests, each memory access request identifying an address in memory to which the request is directed;

at least one on-chip resource falling within the address space addressable by the processor;

an interface for directing packets off-chip and addressable within the address space of the, processor;

a request directing unit for receiving said memory access requests and directing them in accordance with a selected one of first and second address maps, wherein said first address map has a first range of addresses allocated to said at least one on-chip resource and a second range of addresses allocated to said interface, and in the second memory address map said first range of addresses are also allocated to the interface; and

an off-chip circuit connected to said interface and including at least one off-chip memory resource, wherein said interface comprises at least one chip-side port for transmitting memory access requests in parallel across a plurality of pins and first and second circuit-side ports each with a reduced number of pins for communicating said packets off-chip.

13. (Previously Presented) A prototype system according to claim 12, which comprises a mode setting pin operatively connected to the request directing unit for selectively setting a first mode in which said first address map is utilized and a second mode in which said second address map is utilized.

14. (Previously Presented) A prototype system according to claim 12, wherein said request directing unit comprises switching circuitry responsive to a mode setting signal for selectively directing the memory access request to one of said first and second address maps.

15. (Previously Presented) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory mapped peripheral.

16. (Previously Presented) A prototype system according to claim 12, wherein said at least one on-chip resource comprises a memory access device connectable to an off-chip memory resource.

Claim 17 (Canceled).

18. (Currently Amended) A prototype system according to claim ~~17~~ 12, wherein said interface comprises circuitry for chopping a packet transmitted on the chip-side port into chunks so as to be transmitted in a plurality of cycles on the reduced number of pins on the first circuit-side port.

19. (Previously Presented) A prototype system according to claim 12, wherein the interface further comprises circuitry for reassembling chunks received in a plurality of cycles on said set of pins at said second circuit-side port into a single packet for transmission via said at least one chip-side port.

Claims 20-26 (Canceled).